AF/ 2822

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

THEODORE W. HOUSTON

Serial No. 10/054,957 (TI-25900.1)

Filed January 25, 2002

For: ASYMMETRICAL DEVICES FOR SHORT GATE LENGTH PERFORMANCE WITH DISPOSABLE SIDEWALL

Art Unit 2822

Examiner Toniae M. Thomas

Customer No. 23494

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Jay M. Cantor, Reg. No. 19,906

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

An appeal is pending in parent application Serial No. 09/368,387.

STATUS OF CLAIMS

This is an appeal of claims 10 and 25, all of the rejected claims. No claims have been allowed and claims 9, 11, 24 and 26 have been withdrawn from consideration and a divisional application for these claims has been filed. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was filed after final rejection and not entered.

SUMMARY OF INVENTION

The invention relates to a transistor which includes, with reference to Figures 4A and 4B, a semiconductor substrate (1) having first and second spaced apart source/drain regions (3, 5) therein and a channel region between the source/drain regions in the substrate having a relatively low V_T central region (27) between the source/drain regions and relatively high V_T regions adjacent to the source/drain regions (29), the channel region having an implanted one of a positive or negative V_T dopant intermediate the source/drain regions and having an implanted one of a negative or positive V_T dopant adjacent the source/drain regions, the opposite of the dopant in the channel region.

As stated in paragraph [0008], as a fourth embodiment (with reference to Figs 4A and 4B), the FET can be made symmetrical rather than asymmetrical as described in the first and second embodiments with a different implant in the center of the channel region relative to the source and drain ends of the channel region. An implant can be performed following sidewall formation. The sidewalls would then be removed and the entire channel region would be doped n- or p-type to provide either a less heavily net doped region adjacent the source and drain

regions if the same conductivity type dopant is used or a more heavily net doped region adjacent the source and drain if the opposite conductivity type dopant is used. The resist pattern used to mask removal of selected sidewalls can also distinguish n- and p-channel transistors for different V_T implants. Optionally, an implant can be performed before formation of the sidewalls, followed by an implant after formation of the sidewalls. For this option, the sidewall can be left in place for formation of the actual gate.

ISSUES

The issues on appeal are as follows:

1. Whether claims 10 and 25 comply with the written description requirement of 35 U.S.C. 112, first paragraph.

2. Whether claims 10 and 25 are definite under 35 U.S.C. 112, second paragraph.

3. Whether claims 10 and 25 are anticipated by Sasaki (U.S. 4,371,955) under 35 U.S.C. 102 (b).

GROUPING OF CLAIMS

The claims stand or fall together.

ARGUMENT

ISSUE 1

Claim 10 and 25 were rejected under 35 U.S.C, first paragraph, as failing to comply with the written description requirement, the rejection alleging that claim 10 refers to the third embodiment and that the specification does not provide support for the claim language "said channel region having an implanted one of a positive of negative V_T dopant intermediated said source/drain regions

and having an implanted one of a negative or positive V_T dopant adjacent said source/drain regions, the opposite of said dopant in said channel region". This allegation is without merit as will be demonstrated and as should be apparent from the Summary of Invention as discussed above with reference to the application as filed.

As stated at page 5, lines 9ff, paragraph [0008] "the FET can be made symmetrical rather than asymmetrical as described in the first and second embodiments with a different implant in the center of the channel region relative to the source and drain ends of the channel region. This means that the channel has a central portion different from the region of the channel adjacent both of the source/drain regions and is the same as the first or second embodiments except that the asymmetry has been changed to symmetry with respect to the regions 29 (Fig. 4B) as opposed to the region 17 (Fig. 1D) or region 23 (Fig. 2C). As stated at page 3, lines 13ff, "[t]he controlling region could have a positive V_T and the rest of the channel could have a negative V_T, ... The same applies for p-channel transistors except for a polarity reversal". It follows that either a positive or a negative implant can be used, depending upon whether n-channel or p-channel transistors are being fabricated as is also well known to even a pedestrian in the art. Also, with reference to Figs. 1A to 1D, it is stated at page 7, lines 4ff, "For an n-channel device (it is understood that all conductivity types will be opposite for a p-channel device),... This again demonstrates that both n-channel and p-channel devices are being covered by the language allegedly not supported by the specification. It is further stated at page 4, lines 15ff, "[i]t should be understood that the high V_T implant can be a counter doping of the low V_T implant with appropriate masking to perform the implants in this manner". Counter doping can only be provided by doping first with a first conductivity type dopant and then doping in the same region with a dopant of opposite conductivity. The specification further states at page 9, lines 1ff, paragraph [0019] ", the FET can be made in a symmetrical rather

than asymmetrical embodiment as described in the first and second embodiments with a different implant 27 in the center of the channel region as shown in FIGURE 4A. Optionally, implant 27 may include a punch-through implant. The sidewalls 11, 13 are then removed and the entire channel region is doped wither n- or p-type to provide either a less heavily net doped region adjacent the source and drain regions 29 if the same conductivity type dopant is used or a more heavily net doped region adjacent the source and drain regions if the opposite conductivity type dopant is used and the opposite characteristic in region 27 as shown in FIGURE 4B. Optionally, the implant in the full channel region can be performed prior to sidewall formation. Fabrication then proceeds in standard manner to complete the device". It follows that there is more than adequate support for the portion of claim 10 allegedly not supported by the disclosure. Claim 25 depends from claim 10 and therefore the same issue is present as to this claim .

ISSUE 2

Claims 10 and 25 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite, the Examiner stating that it is not clear, in the clause in claim 10 discussed in connection with Issue 1. which portion of the channel region the phrase "said channel region" refer to: the region intermediate the source/drain regions, or the regions adjacent the source/drain regions. The rejection is without merit.

Claim 10 very clearly states that it includes "a channel region between said source/drain regions in said substrate". This means that the entire channel region is disposed between the source/drain regions as is standard and elementary in semiconductor technology. Claim 10 goes on to state "having a relatively low V_T central region between said source/drain regions and relatively high V_T regions adjacent to said source/drain regions". This very clearly means that

the channel region has a relatively low V_T region in the central portion of the channel which is redundantly stated to be between the source/drain regions and relatively high V_T regions adjacent to the source/drain regions, or, otherwise stated, between the central region and the source/drains. This language is clear and unambiguous.

ISSUE 3

Claim 10 and 25 were rejected under 35 U.S.C. 102(b) as being anticipated by Sasaki (U.S. 4,371,955 B1). The rejection is without merit.

Claim 10 requires, among other features, a channel region between the source/drain regions in the substrate having a relatively low V_T central region between the source/drain regions and relatively high V_T regions adjacent to the source/drain regions, the channel region having an implanted one of a positive or negative V_T dopant intermediate the source/drain regions and having an implanted one of a negative or positive V_T dopant adjacent the source/drain regions, the opposite of the dopant in the channel region as discussed above. This claim refers to the fourth embodiment as discussed on pages 5 and 9 of the specification. No such features are taught or suggested by Sasaki either alone or in the total combination as claimed.

A review of Sasaki at column 3, lines 16ff indicates that the semiconductor layer 21 is p-type (line 18) and boron, which is a p-type dopant; is implanted into the regions 211b' and 211c' (lines 22ff). It follows that the regions 21, 211a, 211b and 211c are all p-type with differing doping levels. This is not a dopant of opposite conductivity type in the central region of the channel relative to the dopant in the regions of the channel adjacent the source/drain regions as

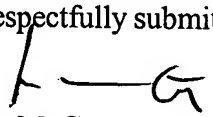
required by claim 10. It follows that claim 10 defines patentably over Sasaki et al. not only under 35 U.S.C. 102 as rejected, but also under 35 U.S.C. 103.

Claim 25 depends from claim 10 and therefore defines patentably over Sasaki for at least the reasons set forth as to claim 10.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,



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APPENDIX

The claims on appeal read as follows:

Claim 10 A transistor which comprises:

(a) a semiconductor substrate having first and second spaced apart source/drain regions therein; and

(b) a channel region between said source/drain regions in said substrate having a relatively low V_T central region between said source/drain regions and relatively high V_T regions adjacent to said source/drain regions, said channel region having an implanted one of a positive or negative V_T dopant intermediate said source/drain regions and having an implanted one of a negative or positive V_T dopant adjacent said source/drain regions, the opposite of said dopant in said channel region.

Claim 25 The transistor of claim 10 wherein said first source/drain region is a source region and said second source/drain region is a drain region.